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09/992,224	11/19/2001	Christopher K. Sutton	10990531-1	5410

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EXAMINER
LAU, TUNG S

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 10/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _05 September 2003_ .

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-24, 26_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-6,8-11,16,18,21,23 and 26_ is/are rejected.

7)☒ Claim(s) _7, 12, 13, 14, 15, 17, 19, 20, 22, 24_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____ .

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4)☐ Interview Summary (PTO-413) Paper No(s). _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____ .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 11, 21, 23, 26, 2, 4, 5, 6, 8, 9, 10, 16 and 18 are rejected under 35

U.S.C. 102(e) as being anticipated by Grey (U.S. Patent Application

2003/0093736).

Regarding claim 1:

Grey discloses an electronic test system for testing an electronic device under

test (DUT), said test system comprising an electronic processor (page 3, section

0052, abstract, fig. 2, unit 160); an electronic memory coupled to said electronic

processor (fig. 2, unit 166); a hierarchical program structure residing in said

memory and executed by said processor (fig. 3, unit 220, page 1-2, section 0018-

0020), said hierarchical program structure having multiple levels including a

measurement level corresponding to a measurement to be performed on said

DUT (page 2, section 0022), lo a test level corresponding to one or more of said

measurements (page 3, section 0052), and a procedure level corresponding to

an ordered list of said tests to be performed on said DUT (page 2, section 0022-
0024).

Regarding claim 3:

Grey discloses an electronic test system for testing an electronic device under
test (DUT), said test system comprising an electronic processor (page 3, section
0052, abstract, fig. 2, unit 160); an electronic memory coupled to said electronic
processor (fig. 2, unit 166); a hierarchical program structure residing in said
memory and executed by said processor (fig. 3, unit 220, page 1-2, section 0018-
0020), said hierarchical program structure having multiple levels including a
measurement level corresponding to a measurement to be performed on said
DUT (page 2, section 0022, fig. 1, unit 150), a test level corresponding to one or
more of said measurements (page 3, section 0052), and a procedure level
corresponding to an ordered list of said tests to be performed on said DUT (page
2, section 0022-0024), each said level embodied in said electronic test system as
a software object (fig. 3, unit 240).

Regarding claim 11:

Grey discloses an electronic test system comprising an electronic processor (fig.
2, unit 160); an electronic memory coupled to said electronic processor (page 3,
section 0052, abstract, fig. 2, unit 160); a hierarchical structure residing in the
memory and executed by said processor (fig. 3, unit 220, page 1-2, section 0018-
0020), said hierarchical structure having multiple levels (page 2, section 0022),
each level embodied in the electronic test system as a function defined by a

class(fig. 4, page 2, section 0026-0027), wherein the implementation of the function is defined by the user of the hierarchical structure by implementing the class (page 2, section 0026-0027); said classes including a measurement class corresponding to a measurement to be performed on said device (page 2, section 0026-0027, page 3, section 0052), a test class corresponding to one or more related measurements (page 2, section 0027-0028), and a procedure class corresponding to an ordered list of tests to be performed on said device (page 2-3, section 0030-0033).

Regarding claim 21:

Grey discloses a method for producing an electronic test system software program for testing an electronic device under test (DUT), said program including a hierarchical structure having multiple levels including a measurement level corresponding to a measurement to be performed on said DUT (page 1-2, section 0018-0022), a test level corresponding to one or more of said measurements (page 3, section 0052), and a procedure level corresponding to an ordered list of said tests to be performed on said DUT (fig. 1, unit 150, page 2, section 0026), each level embodied in said program as a software object for testing a device under test (DUT) (fig. 3, section 240), said method comprising the steps of providing a set of functions wherein the implementation of the functions is defined by said hierarchical structure (page 2, section 0019-0021); implementing the functions to define said test system software program (fig. 4-6); generating said electronic test system software objects by implementing said

functions (fig. 3, unit 240, page 2, section 0021-0027); and utilizing said software

objects to test said DUT (fig. 3, unit 240).

Regarding claim 23:

Grey discloses a computer-readable medium on which is stored a program for

testing an electronic device under test (DUT) (fig. 1, unit 150), 102), said

computer program comprising a measurement software object corresponding to

a measurement to be performed on said DUT (page 1-2, section 0018—0021); a

test software object defining a test algorithm utilizing parameters provided by

said measurement object and corresponding to a test to be performed on said

DUT (page 1-2, section 0018-0021); a procedure software object corresponding

to an ordered list of said tests to be performed on said DUT (page 2, section

0026-0029); and a plurality of software pointers linking said measurement object,

said test object (fig. 3, unit 240, 232), and said procedure object (fig. 3, unit 240,

page 5, section 0068-0072).

Regarding claim 26:

Grey discloses an electronic test system for testing a device under test (DUT),

said test system comprising an electronic processor (fig. 2, unit 160); an

electronic memory coupled to said electronic processor (fig. 2, unit 166); a

procedure residing in said memory and executed by said processor (fig. 3, unit

202, page 2, section 0019-0022), said procedure embodied in the electronic test

system as a software object for testing a device under test (DUT) (fig. 1, unit 150,

page 2, section 0019-0023)), wherein the procedure comprises a function

defined by a class (page 2, section 0027-0030), wherein the implementation of the function is defined by the user of the test system by implementing the class page 2, section 0025-0027, fig. 4); the procedure object including: a first set of software object methods in the procedure object to perform a plurality of predetermined functions to implement said procedure object (fig. 3, 4), test class defining a test object corresponding to a test to be performed on DUT (page 3, unit 0052), a second set of object methods for creating the test and procedure object containing the test object (page 5, unit 0070, page 8, unit 0116).

Regarding claim 2, 4, 5, 6, 8, 9, 10, 16 and 18:

Grey also disclose An electronic test system wherein said hierarchical program structure further includes a datapoint level corresponding to a single result of a measurement, and said measurement level includes a plurality of said datapoints (page 8, section 0116); an electronic test system wherein said hierarchical program structure further includes a datapoint level, and said measurement level corresponds to a group of said datapoints, said datapoint level embodied in said electronic test system as a datapoint software object (page 8, section 0116, fig. 3); An electronic test system wherein said hierarchical program structure further includes a product model level corresponding to a set of procedures for testing a family of said DUT (page 5, section 0070); an electronic system wherein said set of procedures in said product model level are stored in a DLL file (page 5, 0069-

0070); An electronic test system wherein said test object defines a test algorithm (page 1, section 0004).

An electronic test system wherein said test algorithm comprises one or more electronic operations defined by software code, and the electronic parameters for said electronic functions are provided by said measurement Io object (page 3, section 0052). An electronic system wherein said test object contains said measurement object, and said measurement object contains said datapoint object (page 8, section 0116, page 3, section 0052).

An electronic test system wherein said electronic processor further is adapted for electronically communicating with said DUT for executing said test software on said DUT and receiving a plurality of electronic outputs from said DUT corresponding to said measurement objects and said datapoint objects (fig. 1, unit 150, page 8, section 0116).

An electronic test system comprising plug-in software code components residing in said memory and providing an interface to other systems (fig. 1, unit 116, 132), 138).

Claim Objections

2.   Claims 7, 12, 13, 14, 15, 17, 19, 20, 22, 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitation of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: prior art fail to teach the object component modal as CPM objects, the class linked to measurement class, capable of beginning and ending the selected process, controlling temperature and humidity, use of a touch pad, Active X Com interface, datapoint which linked to measurement objects, a second set of object methods for creating a test and procedure object containing test object. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

3. Applicant's arguments filed 9/5/2003 have been fully considered but they are not persuasive.

A. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a measurement level corresponding to a measurement to be performed') are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

B. Applicant argues that the prior art does not show the 'datapoint level', Grey shows the 'datapoint level' in page 8, section 0116, the example given in section 0116 shows different 'datapoint level' in stacker pointer (i.e. pointer in MFC, a NULL object, etc).

C. Applicant argues that the prior art does not show the as a 'function define by class...said class including a measurement class corresponding to a measurement to be performed.. a test class corresponding to one or more related measurement'; Grey discloses 'function define by class...said class including a measurement class corresponding to a measurement to be performed.. a test class corresponding to one or more related measurement' in (page 2, section 0022), (fig. 4, page 2, section 0026-0028), page 3, section 0052), (page 2-3, section 0030-0033).

D. While the meaning of claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allowed. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Note: Applicant should have amended claim 22 in condition for allowance as indicated the previous action (claim 26 is depend on 22).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hierarchical on a DUT approach is common in the art as disclose by Hansen (U.S. Patent 6,449,744) and (U.S. Patent 6,128,759) show on his invention related to method and apparatus for generating a Hierarchical use on a DUT.

5. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tung S Lau whose telephone number is 703-305-3309.

The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, John Barlow can be reached on 703-308-3126. The fax phone numbers for

the organization where this application or proceeding is assigned are 703-308-5841 for

regular communications and 703-308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is 703-308-0956.

TC2800 RightFAX Telephone Numbers : TC2800 Official Before-Final RightFAX - (703)

872-9318, TC2800 Official After-Final RightFAX - (703) 872-9319

TC2800 Customer Service RightFAX - (703) 872-9317

TL

BRYAN BUI
PRIMARY EXAMINER